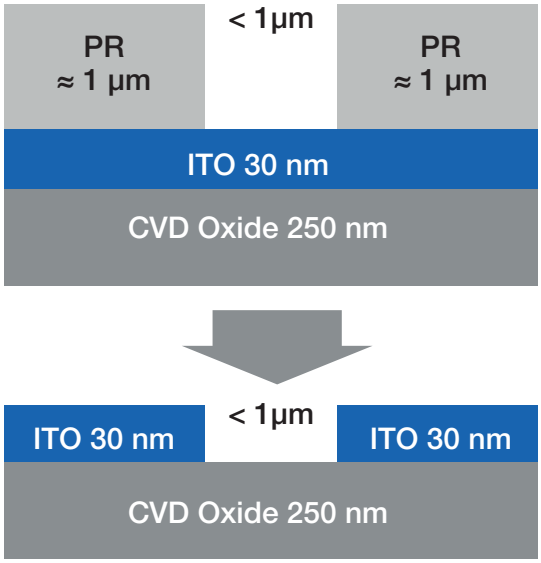
ITO DEP & ETCH ENABLING OLED ON CMOS

Evatec Product Marketing Manager **Franz Xaver Lenherr** tells us how leveraging 30 years of know-how in sputtering and etch helped us fast track development of ITO deposition and ITO etch processes to produce the anode for next generation OLED on CMOS on 300mm.

Meeting demanding specifications

Evatec's new ECL competence lab was created as an environment to work together with customers helping them solve process problems. In this case our customer needed improved ITO sputter deposition and etch processes for the next generation of OLED on CMOS display technology on 300mm substrates. Scientists from the "Solutions Design" team and the process development group of Evatec's Optoelectronics Business Unit joined forces with our ECL lab team to face the challenge using CLUSTERLINE® 300 equipped for 300mm applications.

The stack design required in this case is illustrated in below.



The process specs given by the customer were tough:

ITO deposition

- Deposition of 30 nm ITO on a CMOS backbone
- Thickness uniformity <3% (range/2mean) on a 300mm wafer
- Transmission @450nm on sapphire of >95%

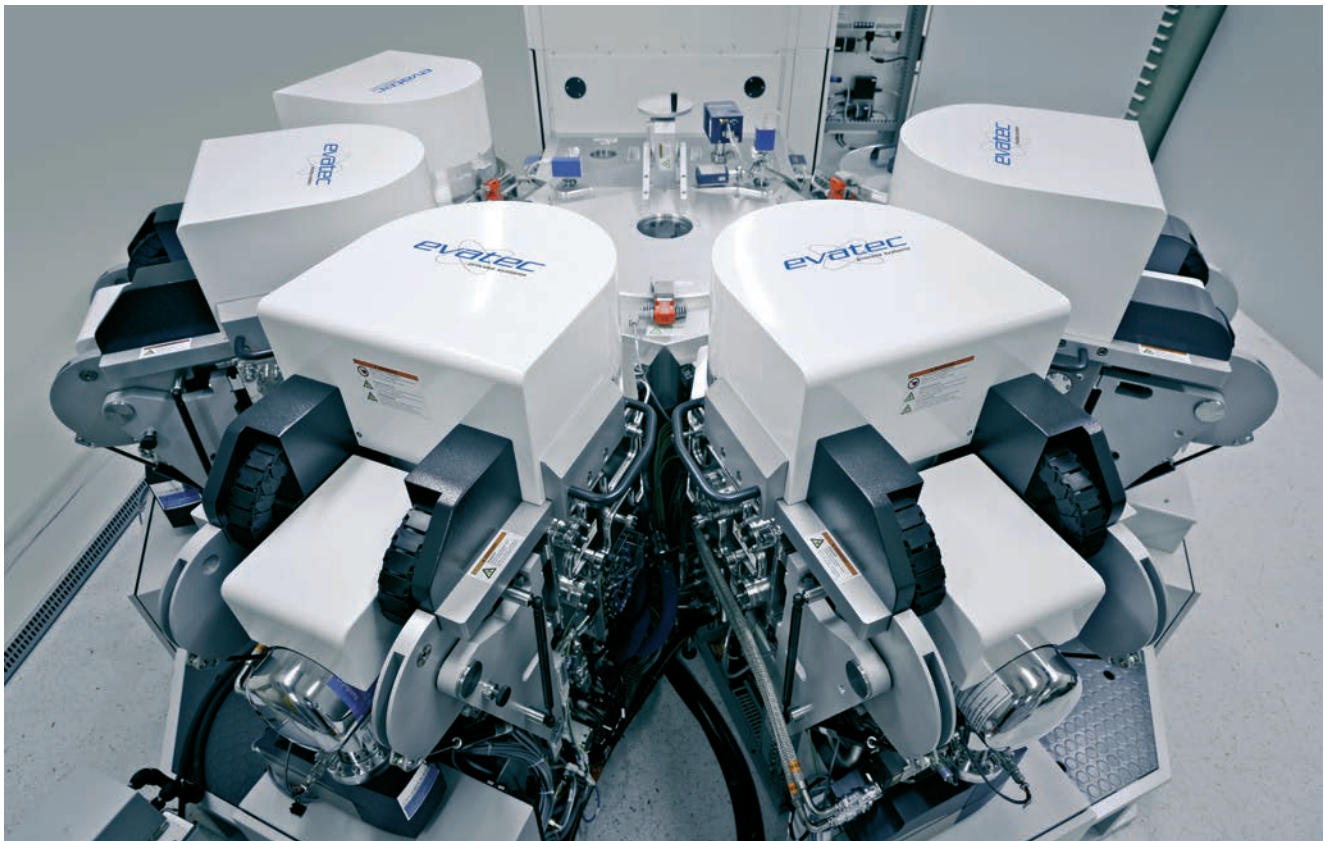
ITO etch

- Etching of 30 nm ITO covered by a thick layer of photo resist (PR)
- Pitch size below 1.0 µm down to 0.4µm
- Underlaying oxide removal <10 nm from an overall thickness of about 250 nm
- Process temperature <150°C.
- Etch rate "as high as possible"
- Uniformity <8% (range/2mean) on a 300mm wafer
- Particle limit >0.2 µm with <30 adders in-film

Process equipment

Both processes were completed on Evatec's CLUSTERLINE® 300 fully automated cassette-to-cassette production platform (figure 1). ITO was produced using the PVD module with its advanced process control features for excellent process uniformity and target utilization, while for the etch process our ICP sputter etch technology combining the use of methane (CH4) with argon (Ar) for reactive ion etching (RIE) was identified as as the ideal solution.

Figure 1. CLUSTERLINE® 300



Why reactive ion etch (RIE) with methane?

Reactive etching with the addition of CH_4 allows selective removal of ITO. This chemically enhanced process only creates volatile compounds like $In(CH_3)x$ and $Sn(CH_3)x$ therefore avoiding any corrosive and hazardous halogen chemistry. Evatec's proprietry ICP sputter etch technology prevents any capacitive coupling to the ICP containment. It features very high plasma density but low damage and good directionality due to independent RF/ICP power process control.

Etch - take a look at the results

We expected particle performance for our process to be good as our chemically enhanced reactive etching process created only volatile compounds, which could be pumped away during the process. Our expectations were met and the process chamber stayed virtually clean over a long period. In particle production tests over 10,000 wafer as shown in figure 2 we could exceed customer expectations by a factor of 3 on average.

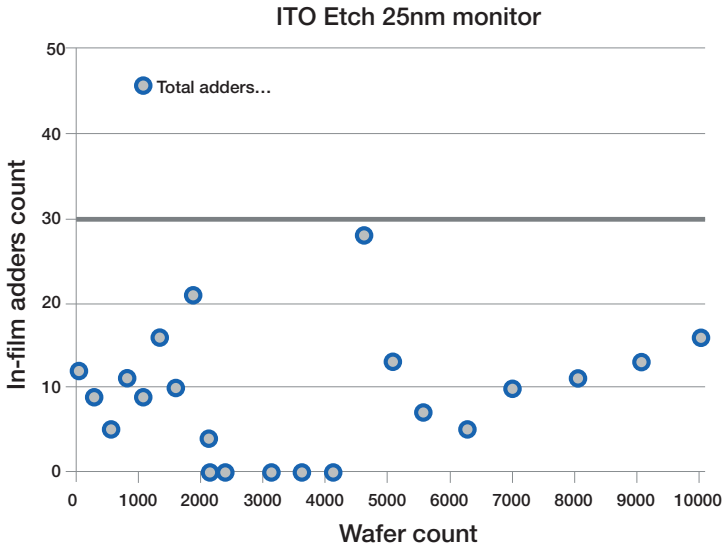


Figure 2. Particle production test over 10,000 wafers

We were also able to demonstrate superior performance in etching the ITO without damage to the underlaying oxide layer. The etch rate for ITO was 2 to 3 times higher than for the oxide below, whilst the very low voltage reduced risk of any surface damage.

The etch process also proved itself to be ideal for production in both precision and repeatability, with the etch rate over 10,000 wafers varying by less than 2.5%. Given a process time of around 35 seconds for the removal of 30 nm and the difference in etching rates between oxide and TCO we were able to stay within the limit for maximum removal of 10 nm of oxide.

Figures 3a to 3d below show very precise pattern etching and virtually vertical sidewalls satisfying our customer requirements.

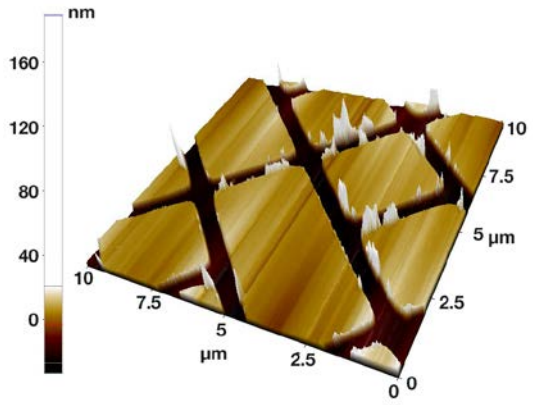


Figure 3a. Perfect etched structure of ITO (peaks are PR not completely removed with manual cleaning

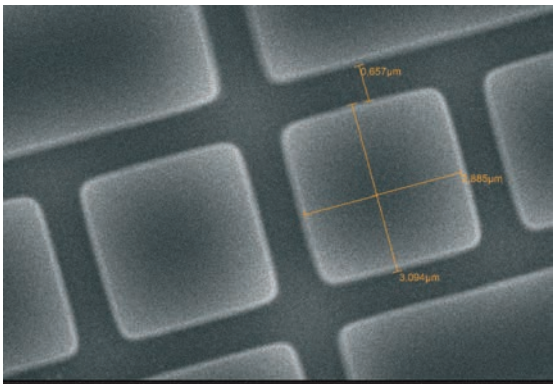


Figure 3b. Pattern before etching

Figure 3c. Pattern after etching

- SEM: no visible damage to PR
- PR: well defined side walls after ITO etching

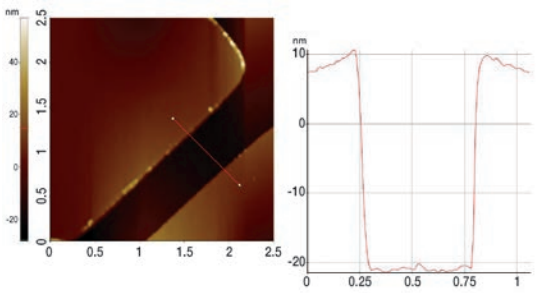


Figure 3d. Pitch of the sidewall after etching. Bottom roughness of <1nm.

When it came to repeatability, a few rounds of process optimization led to results exceeding our customer's expectations and our team was able to demonstrate not only repeatable WiW values of <6.8% (range/2mean), but also WtW values of <5% (range/2mean).

Success thanks to a team effort:

Working as a team together with colleagues from Solutions Design, the Business Unit and ECL was a perfect way to help us fulfil all the customer's baseline requirements. After finishing process development, our process performance exceeded our customer expectations by up to a factor of 3. The production solution was now successfully handed over to the customer for further development and prototyping of next generation devices of OLED on CMOS.

How do we calculate uniformity?

Wafer-in-Wafer: $WIW = \frac{\theta_{max} - \theta_{min}}{2\bar{\theta}}$

Symbols

θ_{max} Max value on wafer

θ_{min} Min value on wafer

$\bar{\theta}$ Average of all values

Overall Results Summary for Deposition and Etch Processes:

Process	Specification	Achieved	Result
ITO dep	Application of 30 nm ITO on a CMOS backbone	Yes	
ITO dep	Thickness uniformity <3% range/2mean	Yes	<1.5% range/2mean
ITO dep	Transmission @450nm on sapphire of >95%	Yes	>97.5%
ITO etch	Pitch size below 1.0µm down to 0.4µm	Yes	
ITO etch	Etching of 30 nm ITO covered by a thick layer of photo resist	Yes	
ITO etch	Underlying oxide removal <10 nm from an overall thickness of about 250 nm	Yes	<10nm
ITO etch	Process temperature <150°C	Yes	
ITO etch	Etch rate "as high as possible"	Yes	
ITO etch	Uniformity <8% range/2mean on a 300mm wafer	Yes	<6.8%
ITO etch	Particle limit >0.2 µm with <30 adders in-film = average	Yes	<15 adders

"THE JOURNEY HAS NOT ENDED HERE – THE TEAM CONTINUES WORKING!"